FIG. 1A PRIOR ART

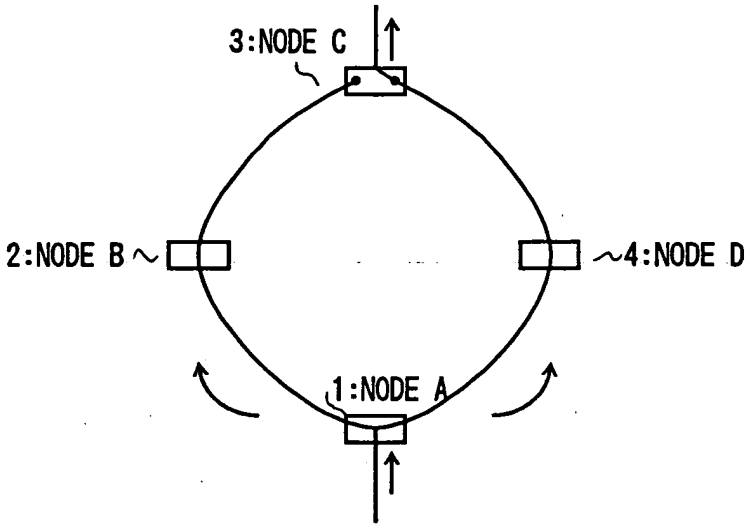


FIG. 1B PRIOR ART

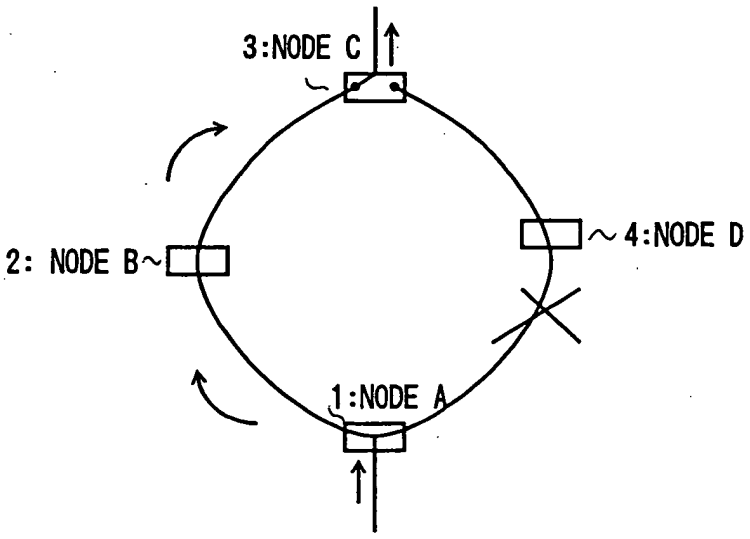


FIG. 2A PRIOR ART

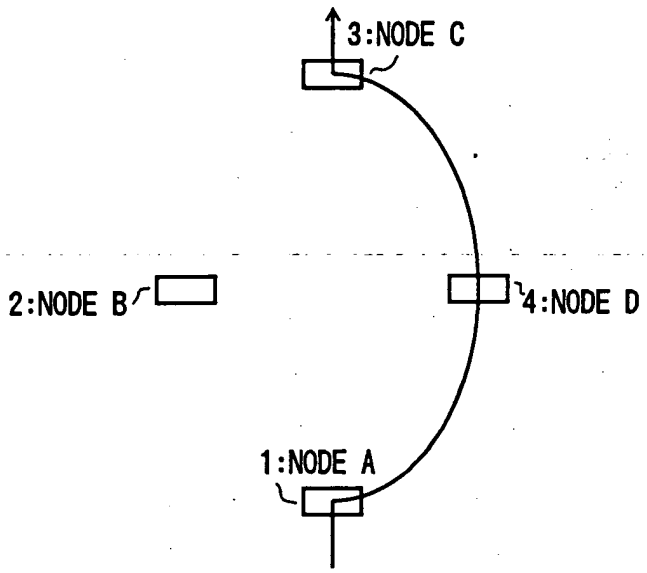


FIG. 2B PRIOR ART

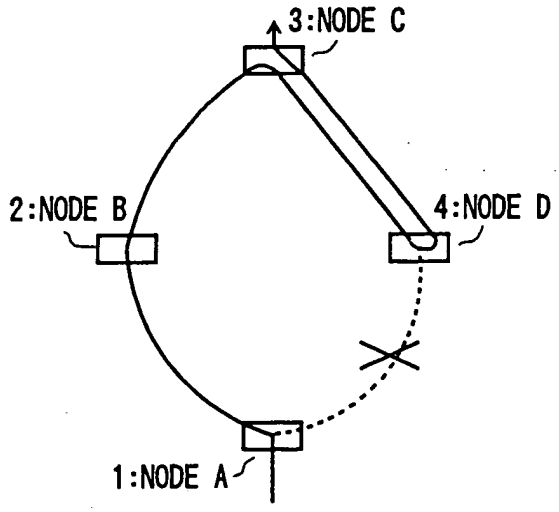


FIG. 3 PRIOR ART

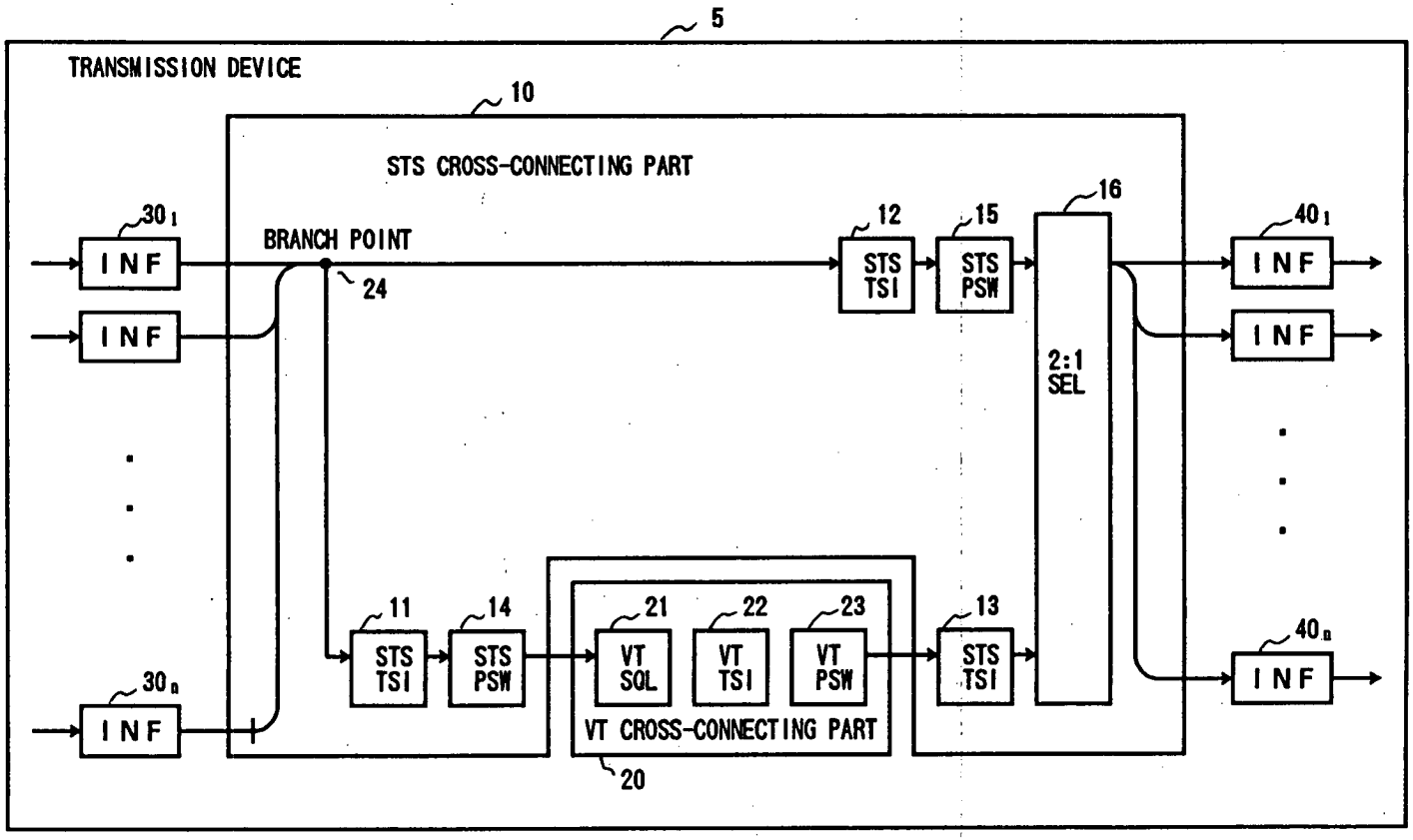


FIG. 4 PRIOR ART

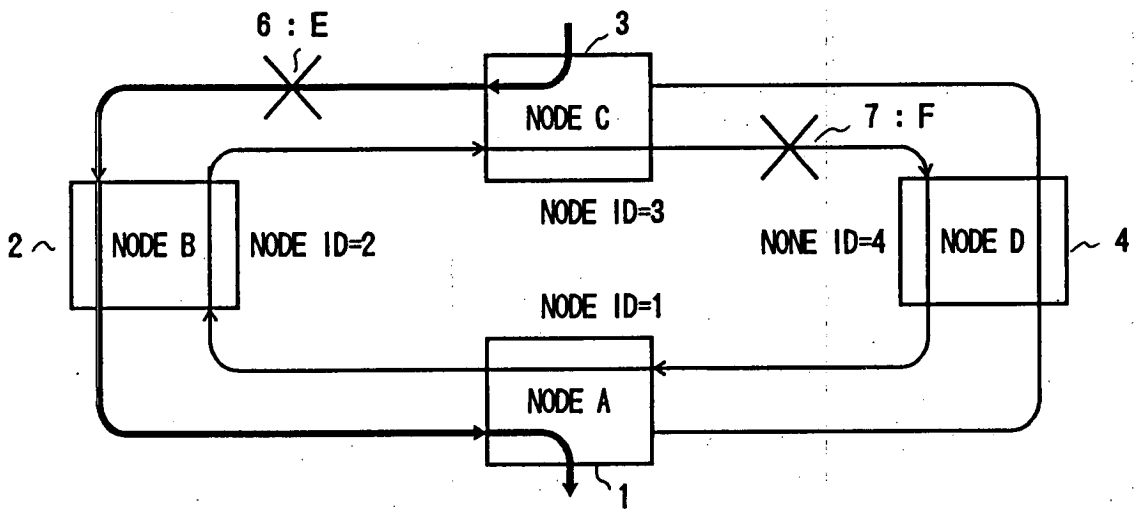


FIG. 5 PRIOR ART

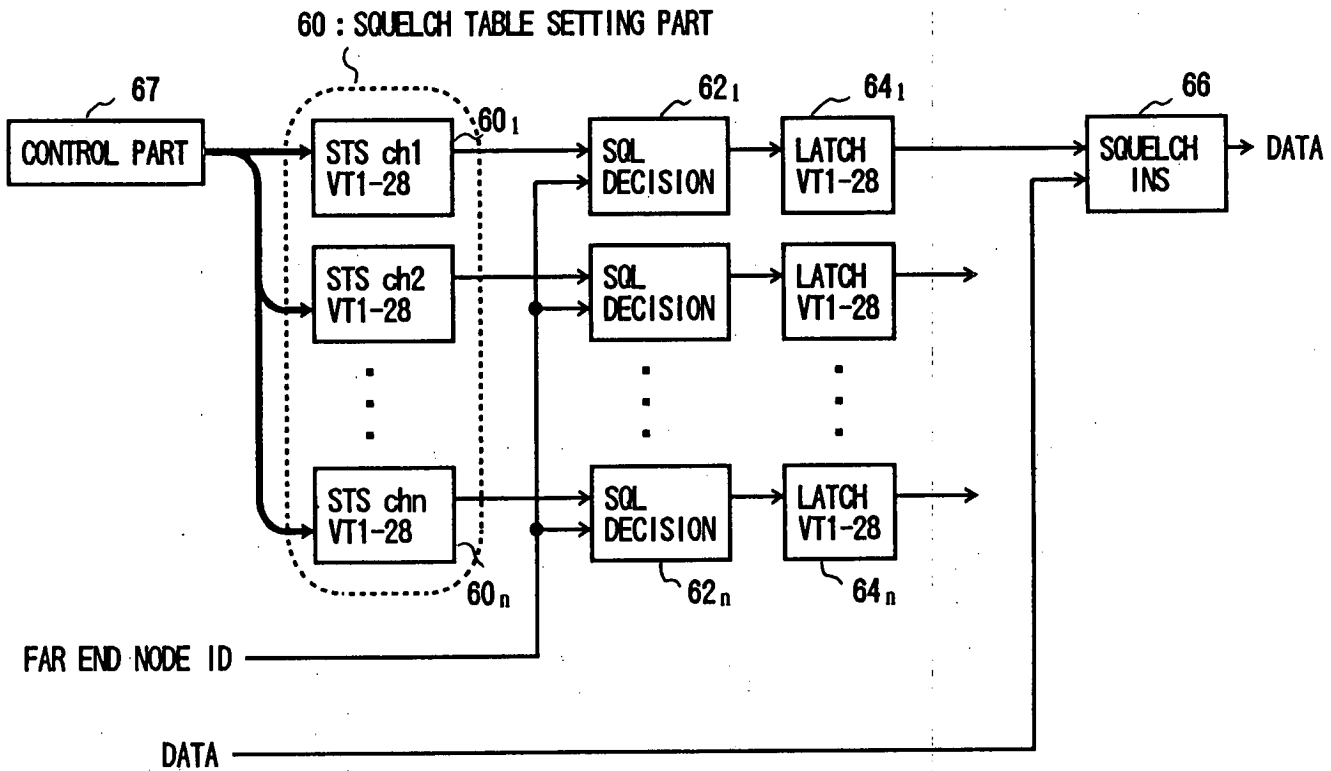


FIG. 6 PRIOR ART

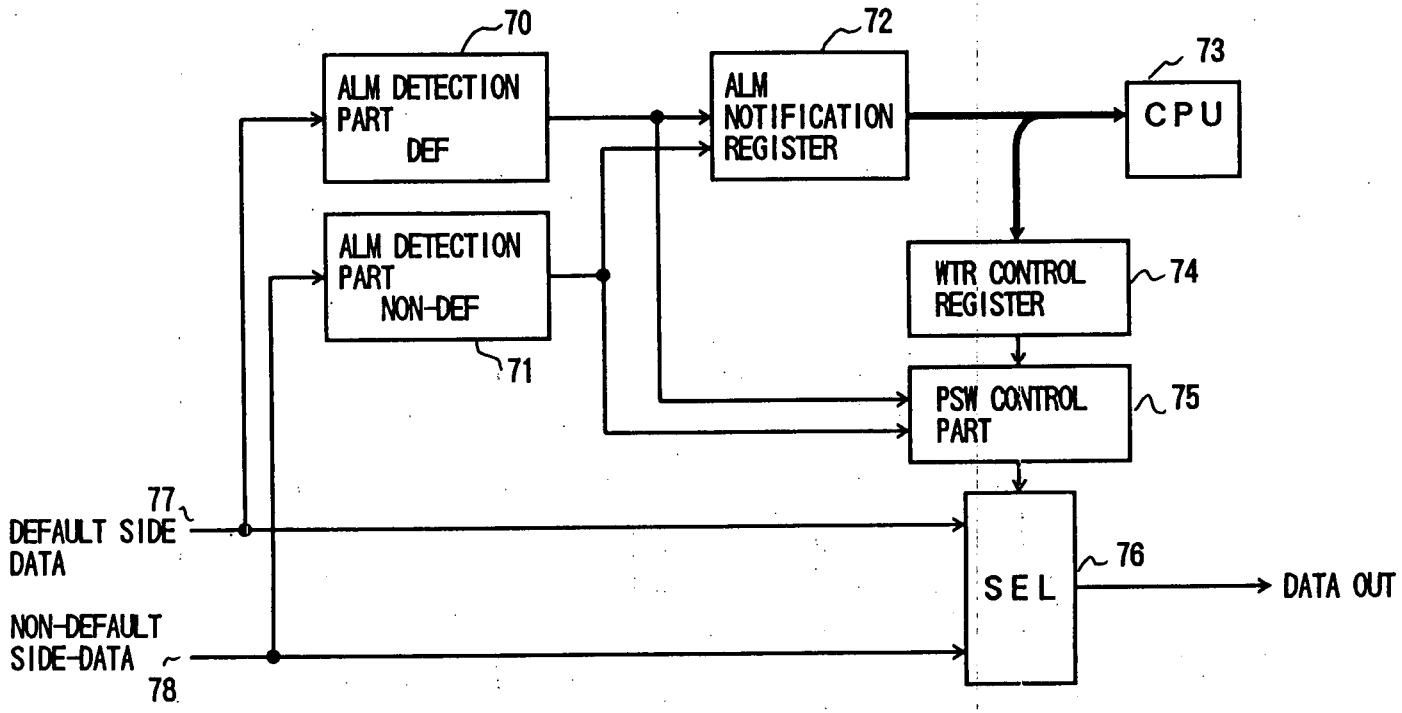


FIG. 7 PRIOR ART

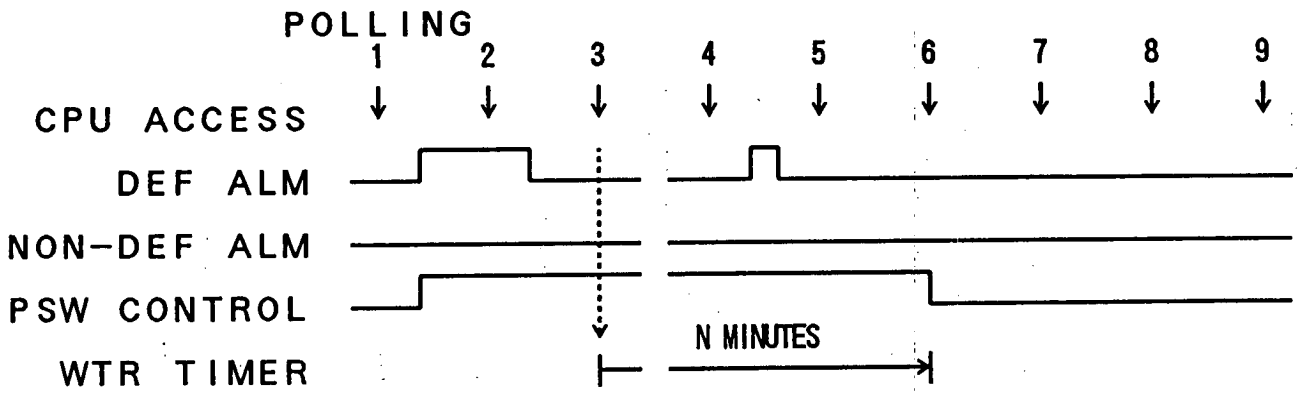


FIG. 8 PRIOR ART

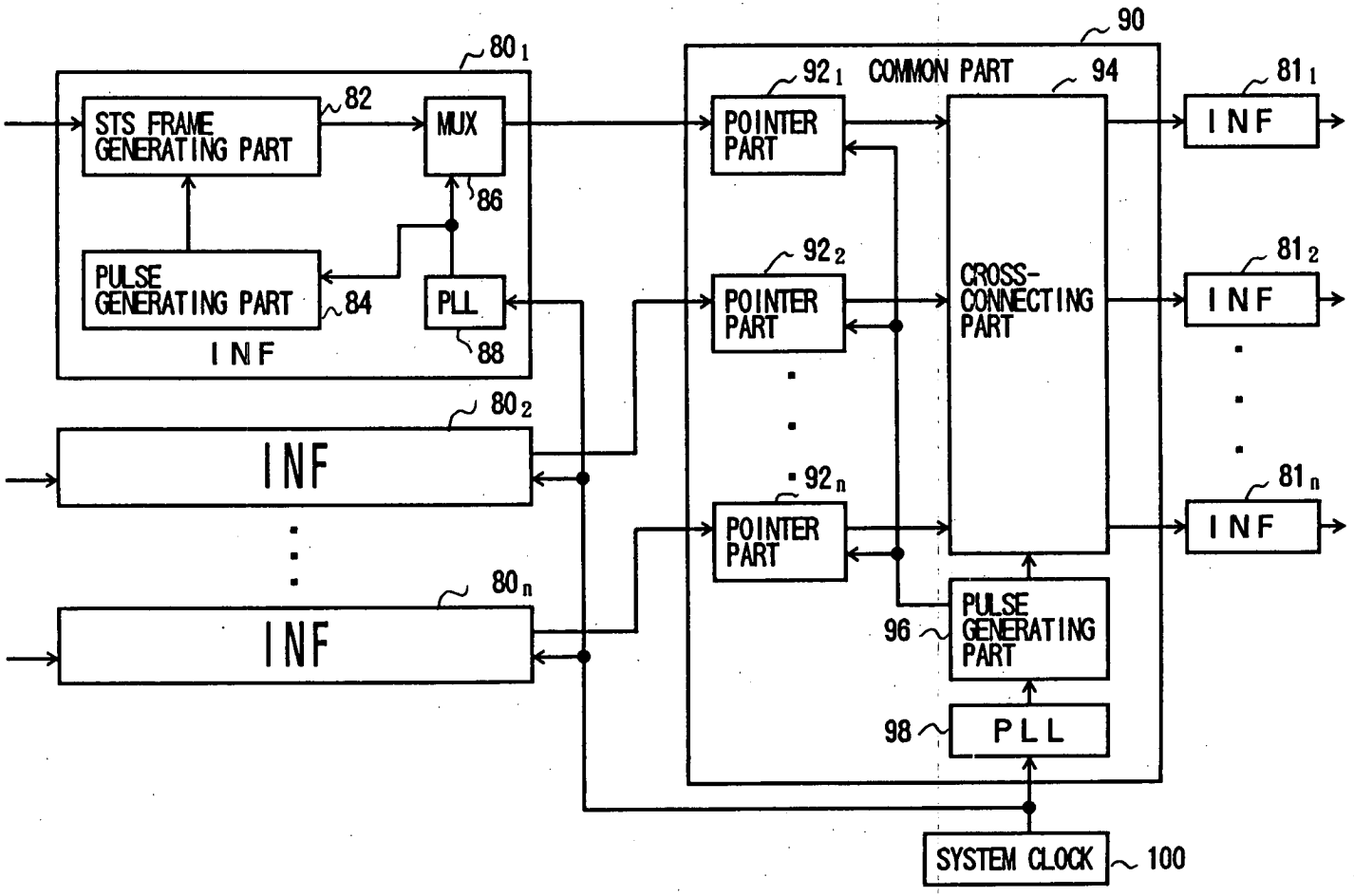


FIG. 9 PRIOR ART

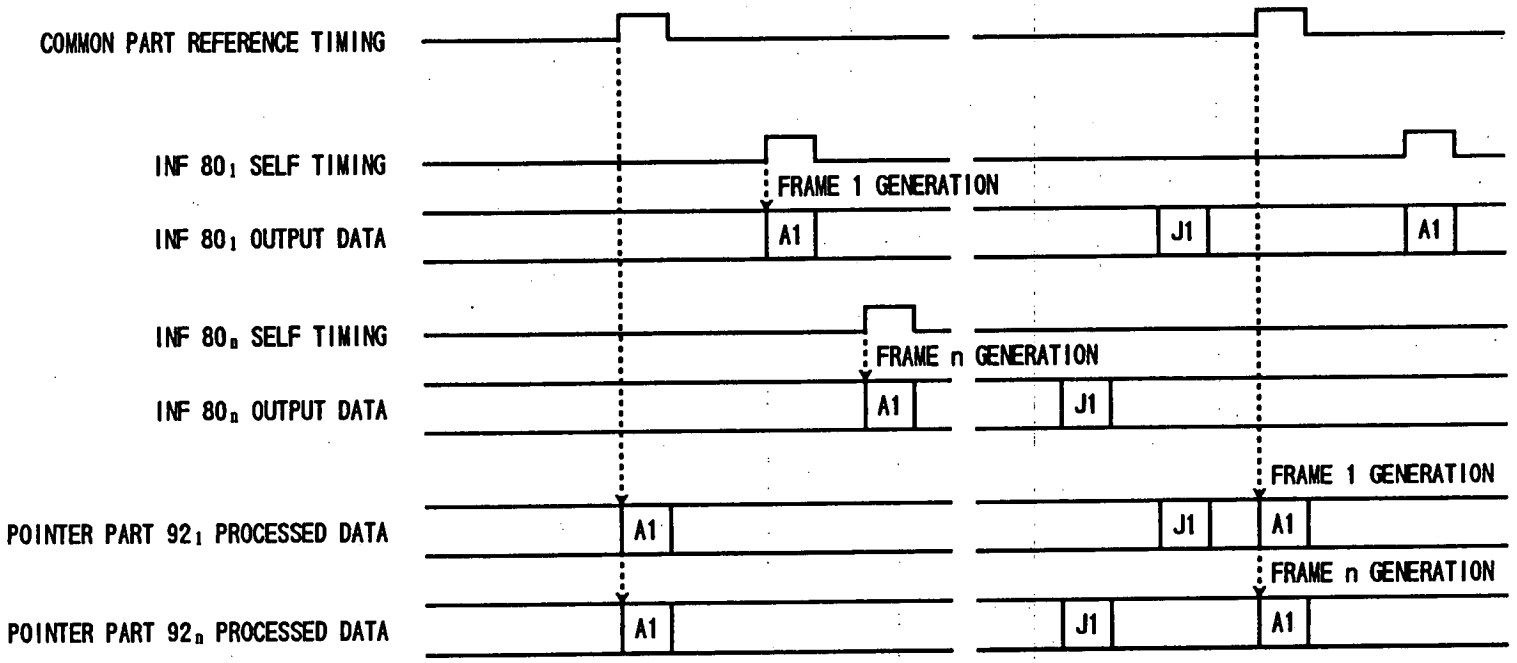


FIG. 10

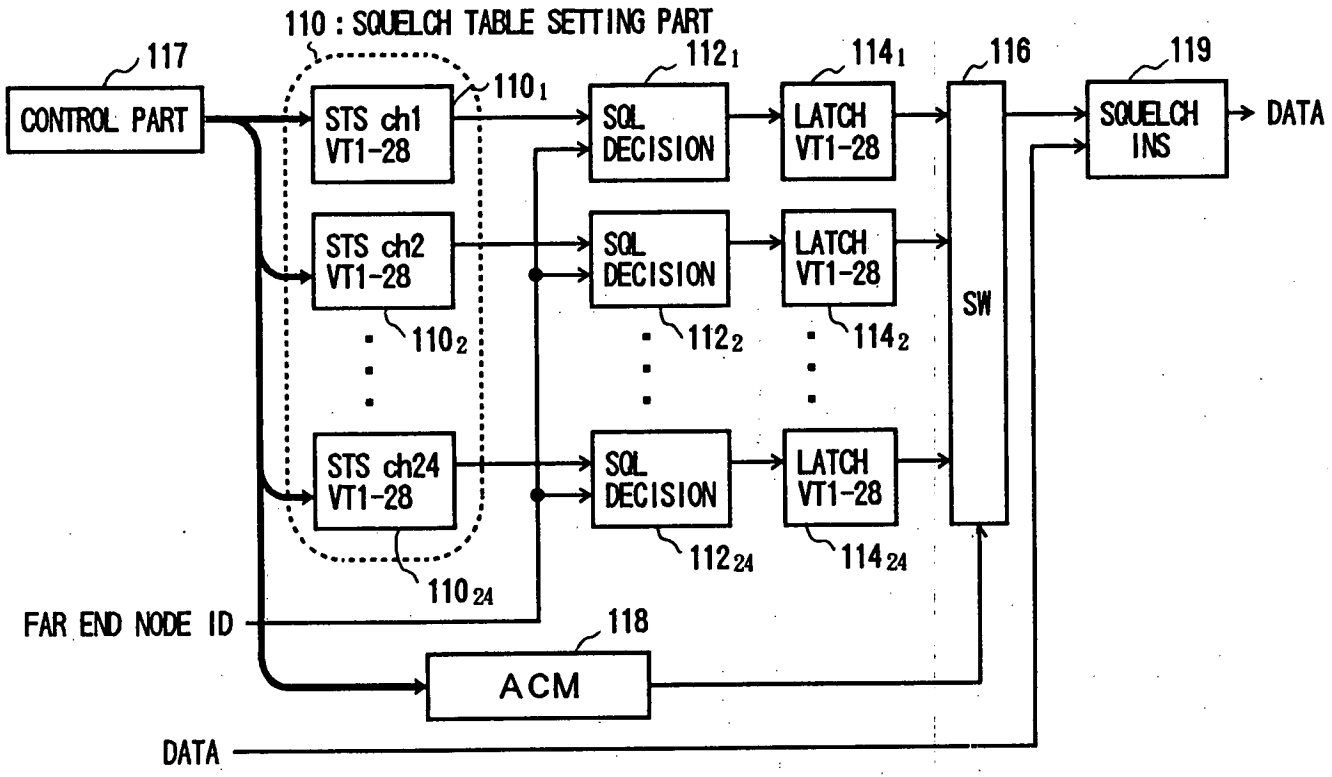

110 : SQUELCH TABLE SETTING PART
117
CONTROL PART
STS ch1 VT1-28
STS ch2 VT1-28
STS ch24 VT1-28
110 1
110 2
110 24
112 1
112 2
112 24
SQL DECISION
SQL DECISION
SQL DECISION
114 1
114 2
114 24
LATCH VT1-28
LATCH VT1-28
LATCH VT1-28
116
SW
119
SQUELCH INS
DATA
FAR END NODE ID
118
ACM
DATA

FIG. 11

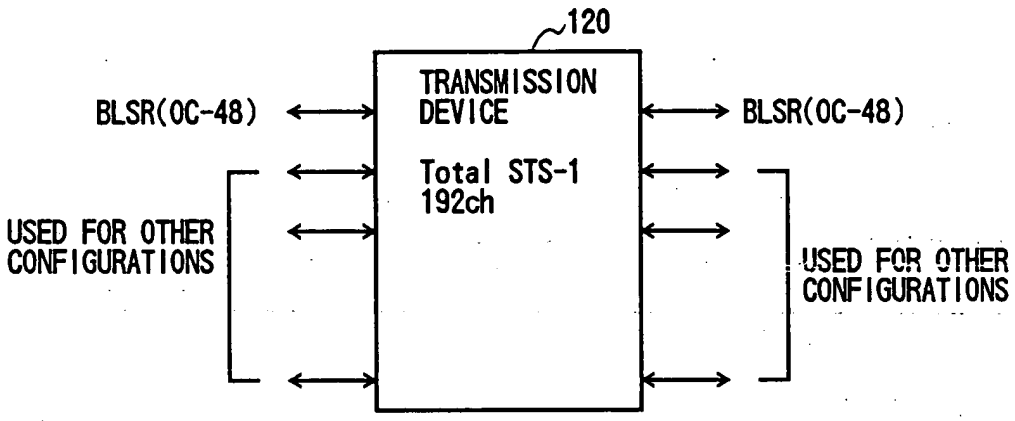

120
TRANSMISSION DEVICE
Total STS-1 192ch
BLSR(OC-48)
BLSR(OC-48)
USED FOR OTHER CONFIGURATIONS
USED FOR OTHER CONFIGURATIONS

FIG. 12

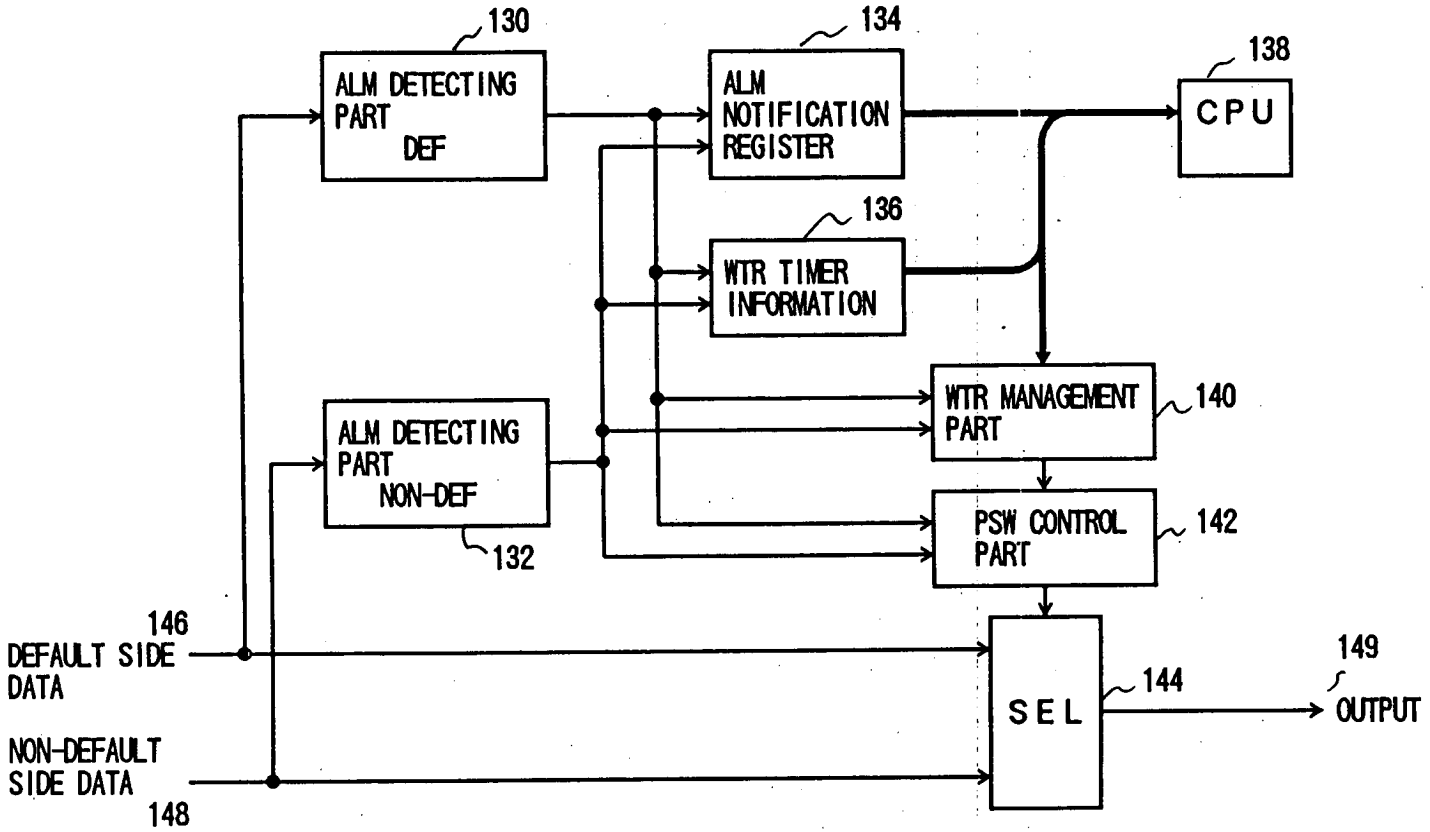

130
ALM DETECTING PART DEF
134
ALM NOTIFICATION REGISTER
138
CPU
136
WTR TIMER INFORMATION
WTR MANAGEMENT PART
140
ALM DETECTING PART NON-DEF
132
PSW CONTROL PART
142
146
DEFAULT SIDE DATA
NON-DEFAULT SIDE DATA
148
SEL
144
149
OUTPUT

FIG. 13

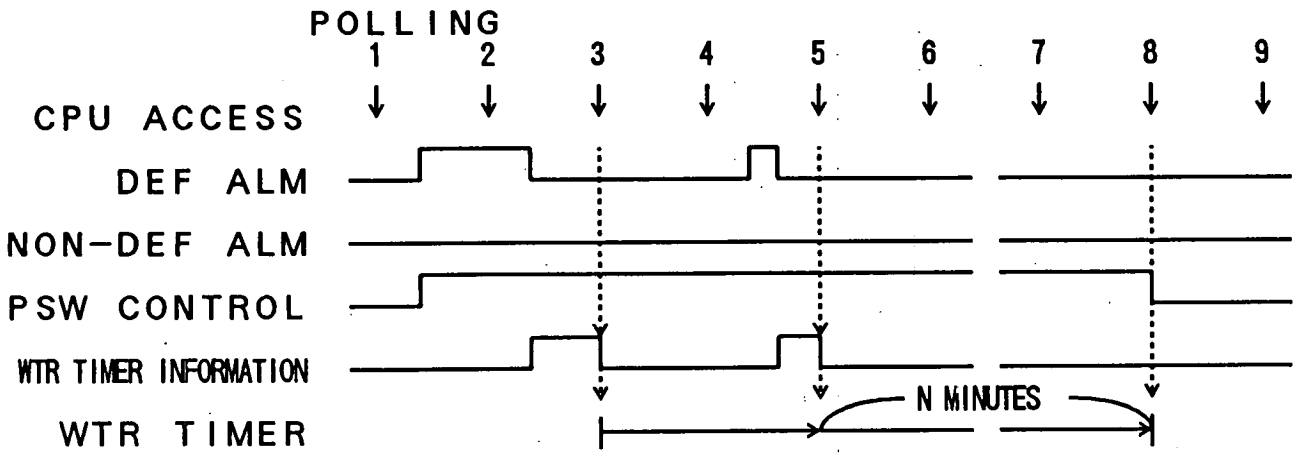

POLLING
1
2
3
4
5
6
7
8
9
CPU ACCESS
DEF ALM
NON-DEF ALM
PSW CONTROL
WTR TIMER INFORMATION
WTR TIMER
N MINUTES

FIG. 14

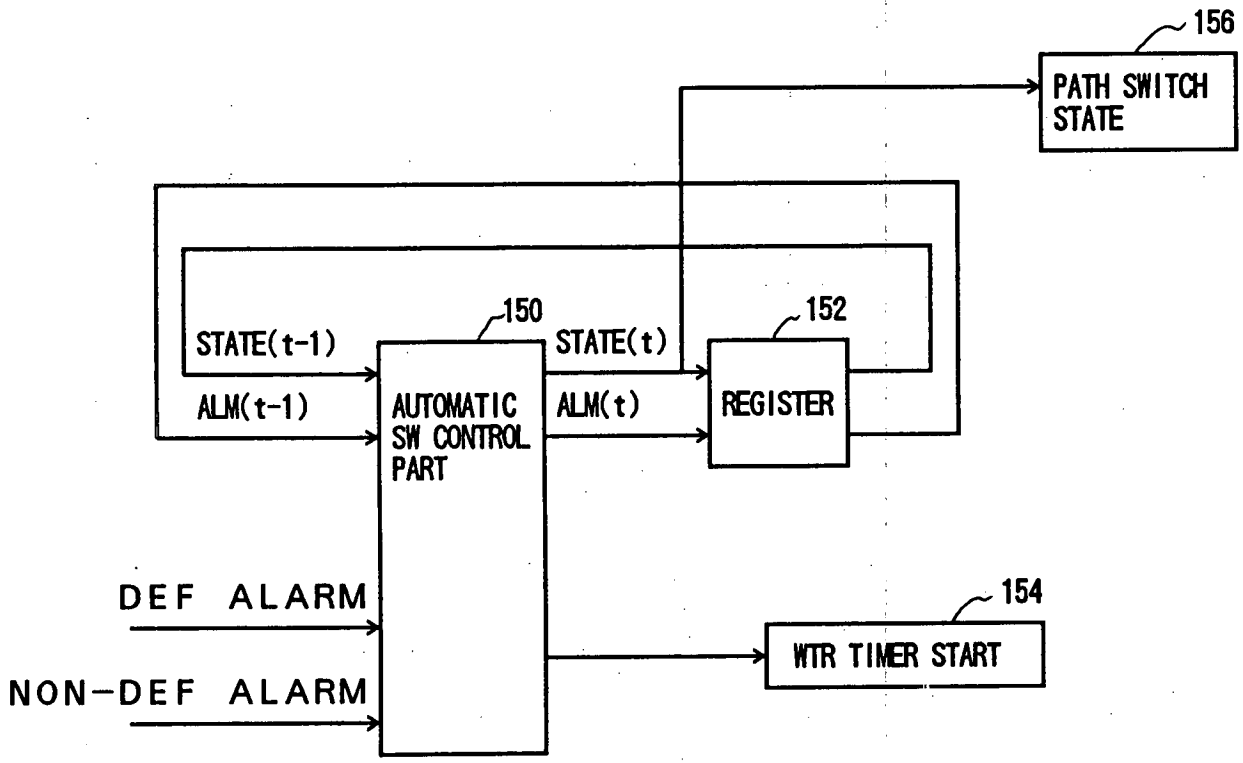

156
PATH SWITCH STATE
STATE(t-1)
ALM(t-1)
150
AUTOMATIC SW CONTROL PART
STATE(t)
ALM(t)
152
REGISTER
DEF ALARM
NON-DEF ALARM
154
WTR TIMER START

FIG. 15

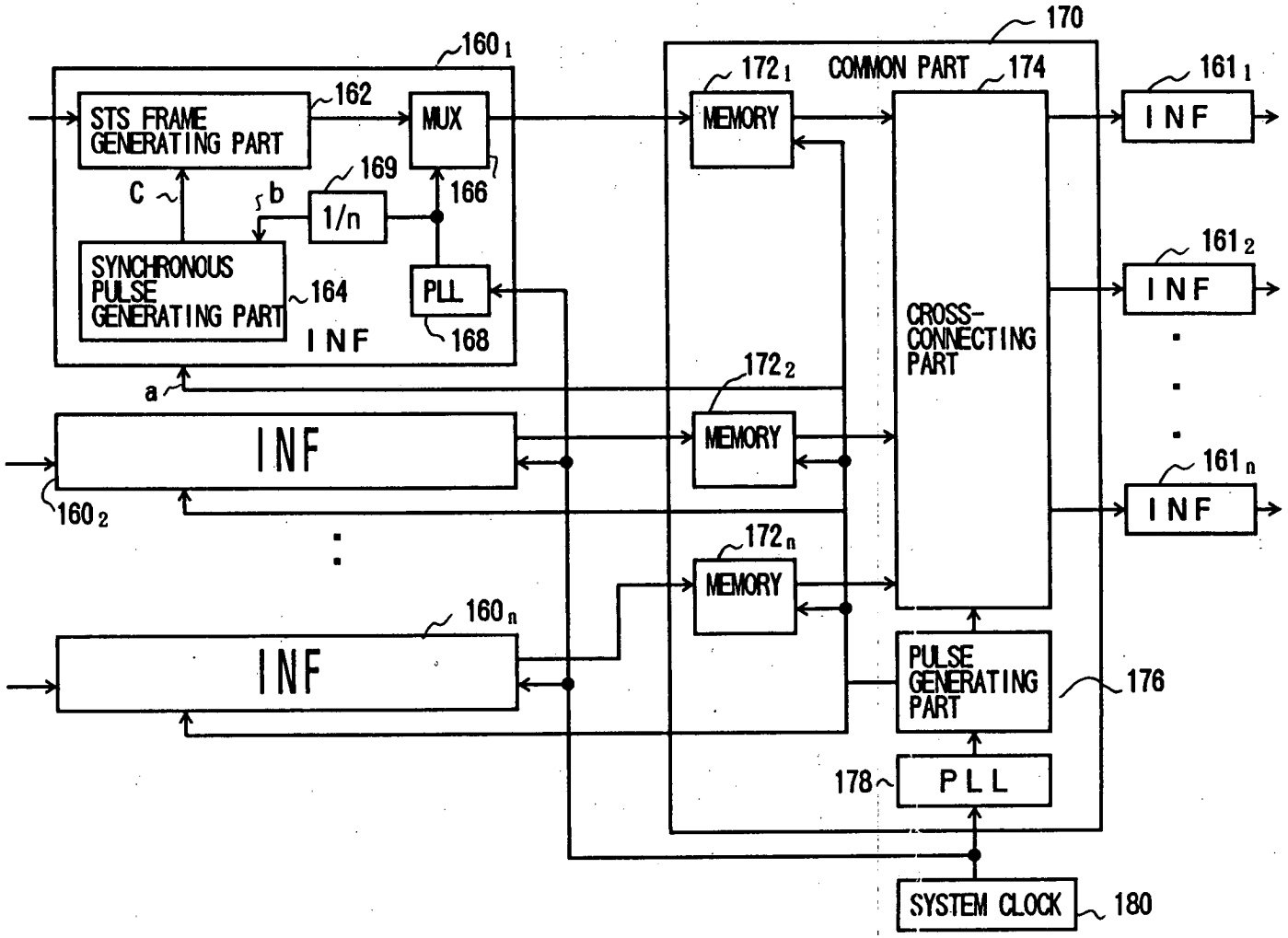

170
160 1
172 1
COMMON PART
174
161 1
STS FRAME GENERATING PART
162
MUX
MEMORY
INF
169
C
b
1/n
166
SYNCHRONOUS PULSE GENERATING PART
164
PLL
168
INF
CROSS-CONNECTING PART
161 2
a
172 2
INF
MEMORY
INF
160 2
161 n
172 n
MEMORY
160 n
INF
PULSE GENERATING PART
176
178
PLL
SYSTEM CLOCK
180

FIG. 16

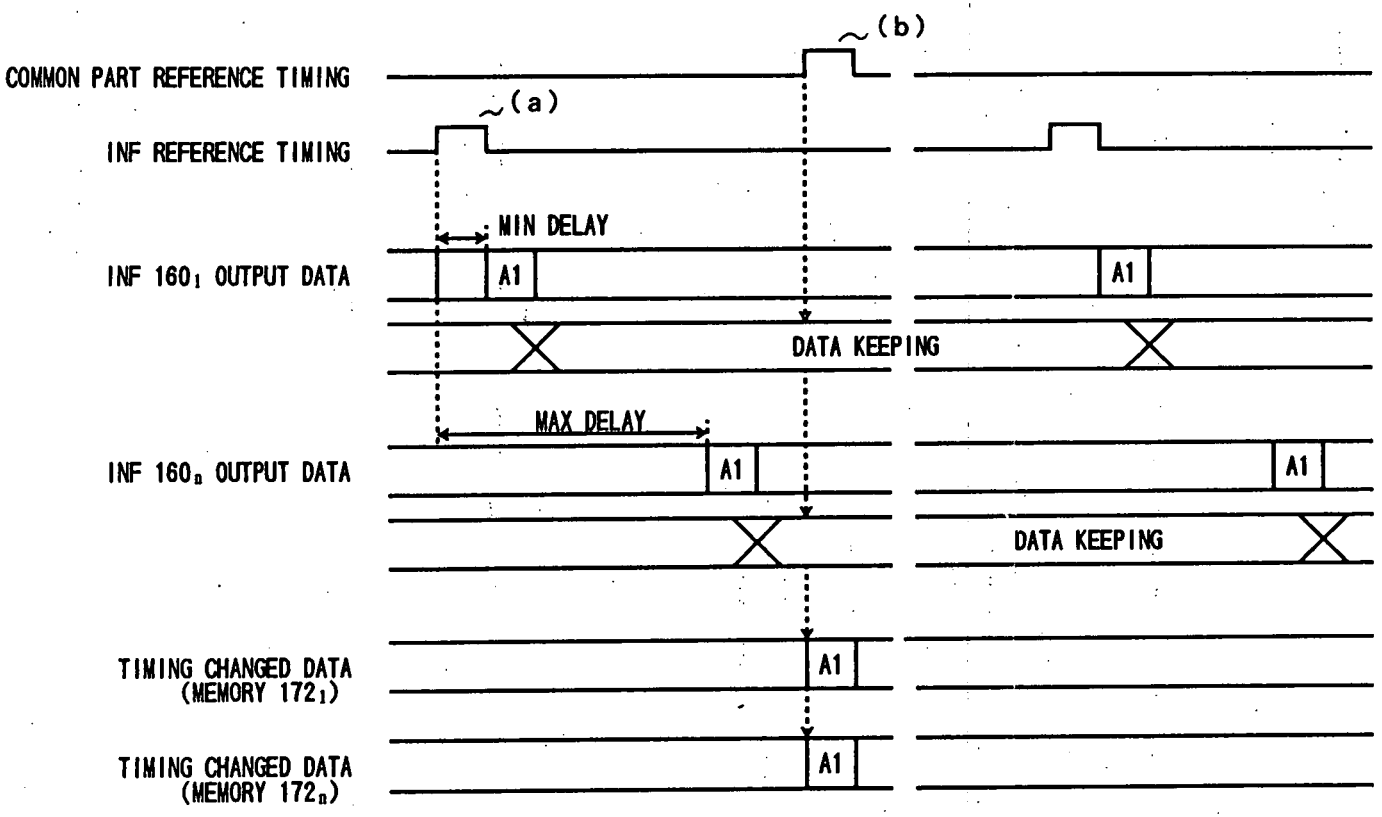

COMMON PART REFERENCE TIMING
INF REFERENCE TIMING
INF 160₁ OUTPUT DATA
INF 160ₙ OUTPUT DATA
TIMING CHANGED DATA (MEMORY 172₁)
TIMING CHANGED DATA (MEMORY 172ₙ)
(a)
(b)
MIN DELAY
MAX DELAY
A1
DATA KEEPING

FIG. 17

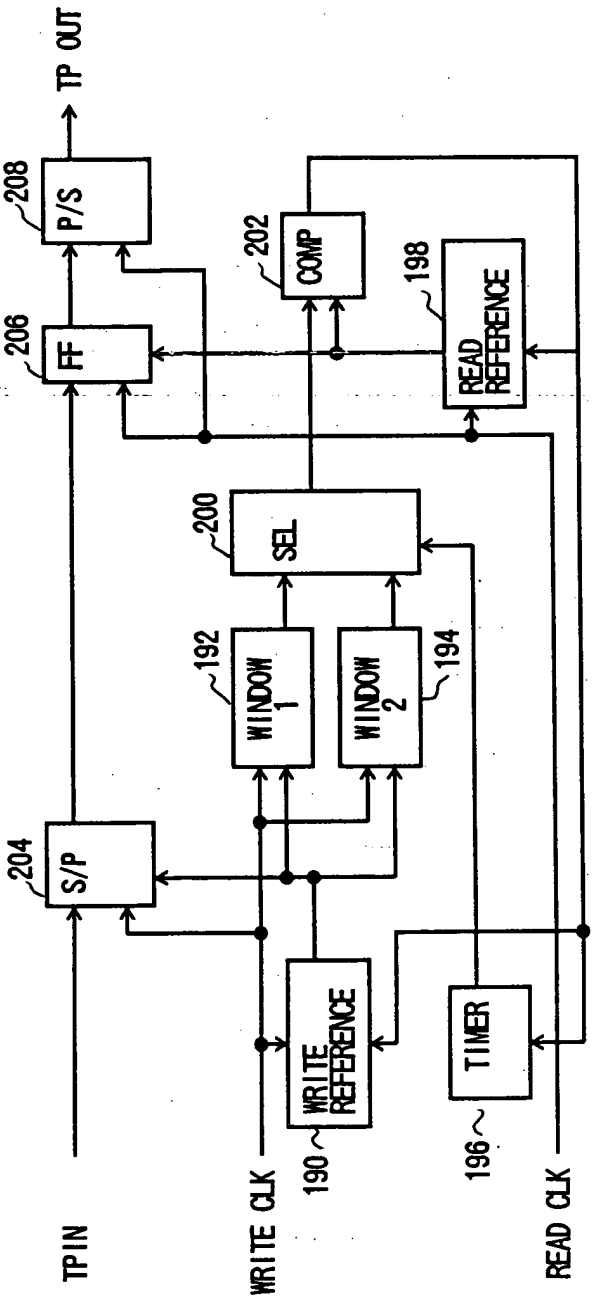

TP IN
WRITE CLK
READ CLK
S/P
204
WINDOW 1
192
WINDOW 2
194
SEL
200
FF
206
P/S
208
TP OUT
COMP
202
READ REFERENCE
198
WRITE REFERENCE
190
TIMER
196

FIG. 18

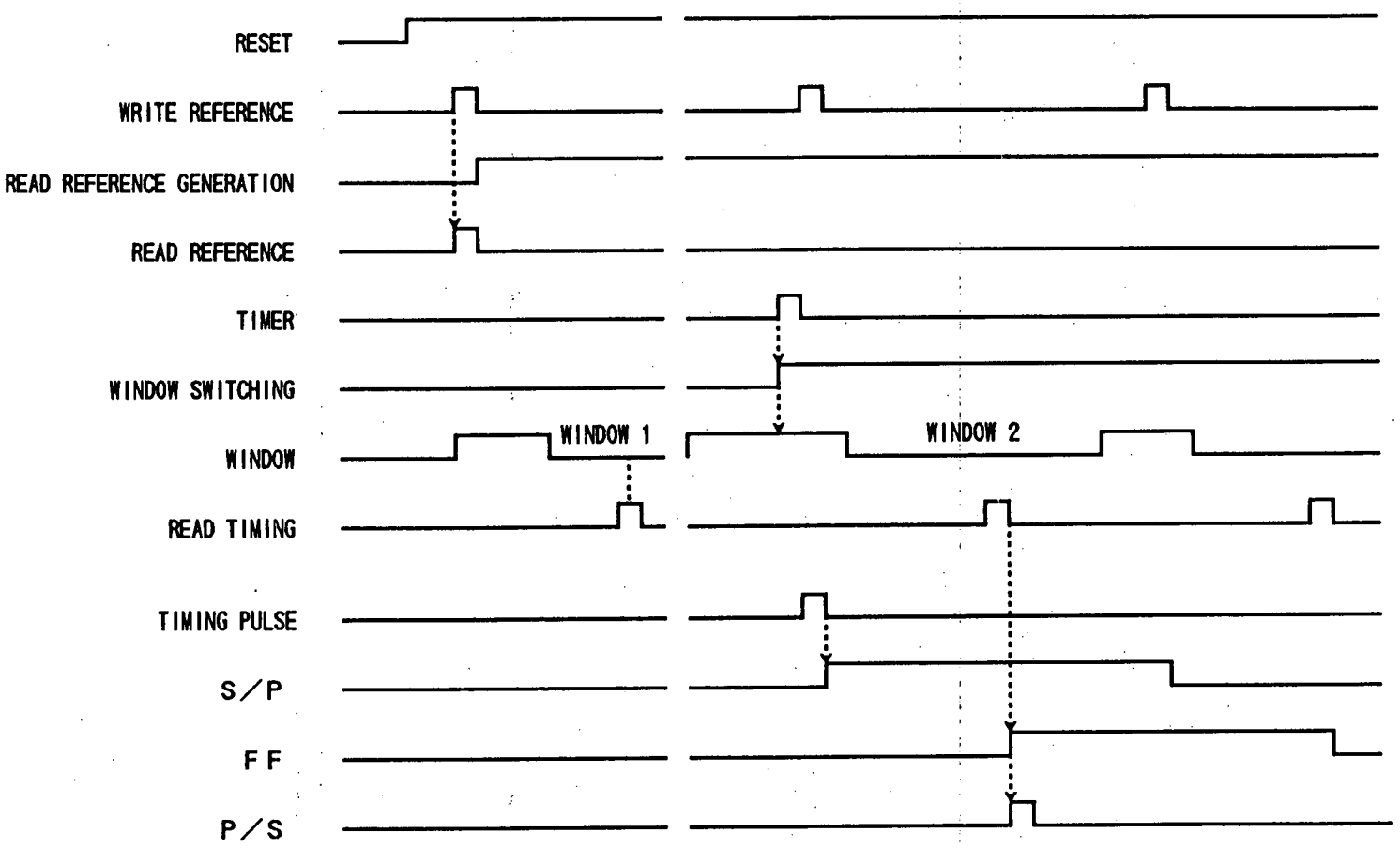
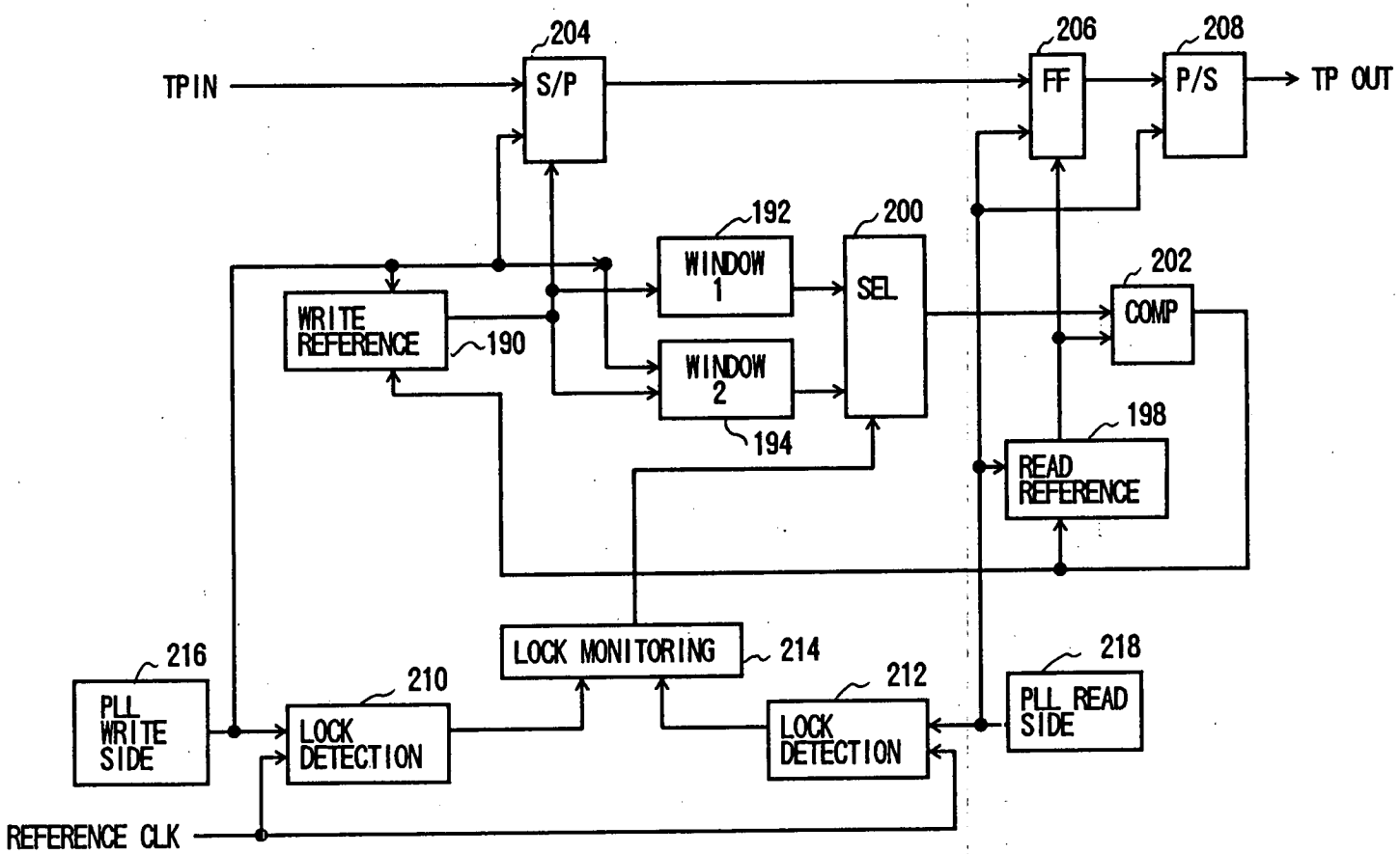

RESET
WRITE REFERENCE
READ REFERENCE GENERATION
READ REFERENCE
TIMER
WINDOW SWITCHING
WINDOW
WINDOW 1
WINDOW 2
READ TIMING
TIMING PULSE
S/P
F F
P/S

FIG. 19


TPIN
204
S/P
206
FF
208
P/S
TP OUT
192
WINDOW 1
200
SEL
202
COMP
WRITE REFERENCE
190
WINDOW 2
194
198
READ REFERENCE
LOCK MONITORING
214
216
PLL WRITE SIDE
210
LOCK DETECTION
212
LOCK DETECTION
218
PLL READ SIDE
REFERENCE CLK